IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Martin Ceredig Roberts et al.	Examiner: Neal Berezny	#7/B Elect. 8/21/01 V. Vannucci
Serial No.:	09/745,780	Group Art Unit: 2823	
Filed:	December 21, 2000	Docket: 303.451US6	
Title:	METHOD FOR FORMING AN INTEGRATED CIRCUIT INTERCONNECT USING A DUAL POLY PROCESS		

RESPONSE TO RESTRICTION REQUIREMENT AND PRELIMINARY AMENDMENT

Commissioner for Patents
Washington, D.C. 20231

#7/B 9/14/01 NB

In response to the Restriction Requirement mailed July 23, 2001, Applicant elects, without traverse, Group II (claims 38-52). Applicant respectfully cancels remaining claims 34-37 (Group I) without prejudice, and reserves the right to reintroduce them in a divisional application at a later date.

Before taking up the above-identified application for examination, please enter the following amendments.

IN THE CLAIMS

Please add the following new claims:

53. (New) The intermediate of claim 38 wherein the first substrate region includes a buried contact region.

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54. (New) The intermediate of claim 38 wherein a portion of the second polycrystalline layer overlying the first polycrystalline layer is removed to expose the first polycrystalline layer and eliminate a horizontal interface between the first and second polycrystalline silicon layers.

55. (New) The intermediate of claim 39 wherein a portion of the second polycrystalline silicon layer overlying the first polycrystalline layer is removed so that a total height of the first polycrystalline silicon layer plus a height of the etch stop layer defines a maximum height of the second polycrystalline silicon layer after removal of the portion of the second polycrystalline